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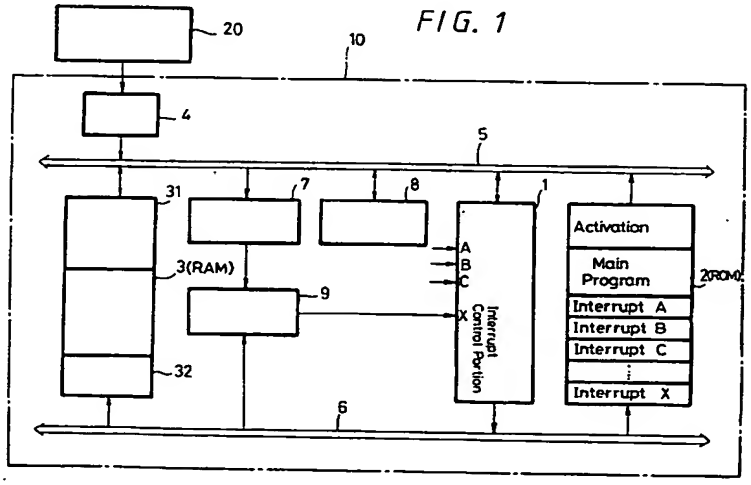
(54) Electronic apparatus and method for patching a fixed information.

(57) An electronic apparatus (10) which includes a CPU (1), a ROM (2), a RAM (3), an input port (4), a data bus (5), an address bus (6), a patching portion address register (7) and a patching interrupt vector register (8) which are connected to the data bus (5), a comparator (9) which compares a coincidence with the address stored in the address register (7) and an address on the address bus (6) and supplies an interrupt to an interrupt control portion of the CPU (1) which is also supplied with other interrupts for other processing. Further, an external storage device (20), connected to the input port (4), supplies a main program bug patching information which is stored in the RAM (3), which includes a stack area (32) in which there are saved data written in the address register (7) and the patching interrupt register (8), so that patching of program bugs can be carried out even during an interrupt.

FIG. 1



EP 0 553 733 A2

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to an electronic apparatus such as a one-chip microcomputer incorporated within electronic devices, for example.

Description of the Related Art:

A one-chip microcomputer incorporated within electronic devices, for example, is formed of an electronic apparatus in which a fixed memory means (ROM (read only memory)), a processing means (CPU (central processing unit)), an input means, a variable memory means (RAM (random access memory)), etc., are unitarily integrated.

In such an electronic apparatus (one-chip microcomputer), a program for the processing in the processing means (CPU) is stored in the fixed memory means (ROM), for example. That is, a particular processing is executed in accordance with an information (processing program) stored in the fixed memory means (ROM). If such fixed memory means is formed of, for example, a mask-ROM, then such electronic apparatus can be made inexpensively by means of mass-production.

The above electronic apparatus are incorporated within electronic devices such as a consumer VTR (video tape recorder) having a built-in camera, a compact video deck or the like. There is a recent trend that the electronic devices (consumer VTRs having a built-in camera or the like) are so designed as to have multiple functions in order to discriminate products. As a result, the amount of information (processing program) stored in the fixed memory means (ROM) is increased and, particularly, the processing program becomes extremely long, which unavoidably causes a defect (bug) to occur.

When such a bug is discovered after the apparatus have been mass-produced, the apparatus which were already mass-produced must be abandoned and the apparatus must be mass-produced one more time. Further, external parts for patching the bug must be mounted on the apparatus. However, a lot of money is needed when the apparatus is mass-produced one more time. Also, it is frequently observed that external parts cannot be substantially mounted on electronic device because various parts were already mounted on the electronic device with high density.

The assignee of the present application has previously proposed a means for patching a bug after the apparatus was mass-produced (see Japanese Patent Application No. 3-118799). According to this previously-proposed application, in the electronic apparatus, there are provided a patch information memory means for patching a bug and an access switching means. A bug portion is discriminated on the basis of an information stored in a fixed memory means. At that bug portion, the memory access is switched from the fixed memory means to the patch information memory means.

In this previously-proposed apparatus, when an information (processing program) stored in the fixed memory means (ROM) is constantly accessed in a predetermined sequential order, if the next patch portion is designated at the end of the processing where an arbitrary patch portion is patched, then a plurality of bug portions can be patched sequentially.

In this previously-proposed apparatus, however, when other, different information is accessed by an interruption or the like, a bug in such different information cannot be patched. More specifically, when a portion to be patched in the first interrupt processing is designated at the beginning of the interrupt processing, for example, the timing at which this interrupt processing itself is executed in the main processing is not specified and the portion to be patched when the interrupt processing is ended becomes different depending on the timing of the interrupt processing. Consequently, the next portion to be patched cannot be designated.

To solve the above problem, according to the prior art, there are provided a patch information memory means and an access switching means for the interrupt processing independently of those of the main processing, whereby a bug can be patched during the interrupt processing. However, this proposal needs many additional circuits. Further, when the interrupt processing is executed in a multiple fashion, there are needed a maximum number of sets of patch information memory means and access switching means, which cannot be effected with ease.

OBJECTS AND SUMMARY OF THE INVENTION

Therefore, it is an object of the present invention to provide an improved electronic apparatus in which the aforesaid shortcomings and disadvantages of the prior art can be eliminated.

It is another object of the present invention to provide an electronic apparatus in which a bug that was discovered after a mass-production can be patched with ease.

It is still another object of the present invention to provide an electronic apparatus in which a bug can be patched during an interrupt processing.

It is a further object of the present invention to provide an improved fixed information patching method in which the aforesaid shortcomings and disadvantages of the prior art can be eliminated.

It is yet a further object of the present invention to provide a fixed information patching method in which a bug that was discovered after a mass-production can be patched with ease.

It is still a further object of the present invention to provide a fixed information patching method in which a bug can be patched during an interrupt processing.

According to a first aspect of the present invention, there is provided an electronic apparatus which comprises a fixed memory means in which an information is stored in a fixed fashion, an address control means for controlling an address, an input means through which an external information is input, a patch information memory means for storing therein a patch information concerning a portion to be changed in the information stored in the fixed memory means, and a switching control means for switching the memory access made by the address control means from the fixed memory means to the patch information memory means. The address control means includes a first memory in which there is saved control data for controlling the switching of memory access by the address control means when an interrupt processing is executed so that the control data for controlling the switching of the memory access during the interrupt processing can be set in the switching control means. The fixed memory means, the address control means, the input means, the patch information memory means and the switching control means being unitarily integrated in the electronic apparatus

According to a second aspect of the present invention, there is provided a fixed information patching method for operation of an electronic apparatus which comprises fixed memory means in which an information is stored in a fixed fashion, address control means for controlling an address, input means through which an external information is input, patch information memory means for storing therein a patch information concerning a portion to be changed in the information stored in the fixed memory means, and switching control means for switching the memory access made by the address control means from the fixed memory means to the patch information memory means at a predetermined address. This method comprises the steps of saving the control data for controlling the switching of the memory access by the address control means to a first memory during the beginning of an interrupt processing to the address control means, and setting the control data for controlling the switching of the memory access during the interrupt processing in the switching control means. The fixed memory means, the address control means, the input means, the patch information memory means and the switching control means are unitarily integrated in the electronic apparatus.

According to the present invention, the information stored in the fixed memory means is patched by the information from the patch information memory means and the information bug that is discovered after electronic devices were mass-produced can be patched. Also, by saving discriminating data of the patch portion to a stack memory, a bug can be patched during the interrupt processing.

The above and other objects, features, and advantages of the present invention will become apparent from the following detailed description of an illustrative embodiment thereof to be read in conjunction with the accompanying drawings, in which like reference numerals are used to identify the same or similar parts in the several views.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing an arrangement of an electronic apparatus according to an embodiment of the present invention;

FIGS. 2A and 2B are diagrams used to explain the processing program, respectively;

FIG. 3 is a diagram used to explain information that should be patched; and

FIG. 4 is a diagram used to explain operation of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention will now be described with reference to the drawings.

In FIG. 1 of the accompanying drawings, reference numeral 10 generally designates a one-chip microcomputer serving as an electronic apparatus. The electronic apparatus 10 includes a CPU (central processing unit) 1 serving as a processing means, a ROM (read only memory) 2 serving as a fixed memory means, a RAM (random access memory) 3 serving as a patch information memory means, an input means 4, e.g. an input/output (I/O) port or the like. The CPU 1, ROM 2, the RAM 3 and the input means 4 are connected to one another via a data bus 5. An address output formed by the CPU 1 is supplied through an address bus 6 to the address inputs of the ROM 2 and the RAM 3.

There are provided a patch portion address register 7 and a patch interrupt vector register 8, respectively. These registers 7 and 8 are connected to the data bus 5. There is provided a comparator 9 which detects a coincidence between the address stored in the register 7 and the address of the address bus 6. The comparator 9 is

connected at its output portion, from which there is obtained a signal representative of the coincidence of the addresses, to an interrupt control portion X of the CPU 1. The CPU 1 includes also interrupt control portions A, B, C, ... for other processing.

An external storage device 20 is connected to the input means 4. The external storage device 20 also is incorporated within the electronic device. The external storage device 20 is formed of an EEPROM (electrically erasable and programmable ROM) in which there are generally stored parameters obtained in the adjustment process of electronic device, etc. An information from the external storage device 20 is supplied through the input means 4 and then stored in the RAM 4, thereby being utilized in the processing done by the CPU 1.

In the above electronic apparatus 10, a program information for the processing in the CPU 1 is stored in the ROM 2 in a fixed fashion. In this processing program, there is provided an activation program shown in FIG. 2A, for example. The activation program includes a program for initializing the apparatus such as when the RAM 3 is cleared, and a program for transferring the information from the external storage device 20 through the input means 4 to the RAM 3 or the like.

In the processing program stored in the ROM 2, there are provided a main program for executing a main processing and interrupt programs for executing a variety of interruptions A, B, C, ... At the beginning of the main program, there is provided a processing program which writes into the registers 7 and 8, respectively, from the fixed table area 31 of the RAM 3, an address of a first bug portion written in the RAM 3 and vector data representative of a starting position of the patch program for patching the first bug portion.

At the beginning of each interrupt program, as shown in FIG. 2B, there is provided a processing in which data written in the registers 7 and 8 are saved in the RAM 3 at its stack area 32 which will be described later on. This processing is followed by a processing in which an address of a first patching portion corresponding to the interrupt and vector data representative of a starting position of a patch program for patching the bug portion of the interrupt are written in the registers 7 and 8, respectively. At the end of the interrupt program, there is provided a processing in which the data saved in the stack area 32 is written again in the registers 7 and 8.

In the external storage device 20, there are stored information used to patch a bug in the information stored in the ROM 2, together with the parameters obtained in the previously described adjustment process. The information used to patch the bug is shown in FIG. 3 and includes an address of a first bug portion corresponding to the main program and the interrupt, vector data representative of a starting position a patch program for patching the first bug portion, and the patch program.

Then, by the processing of the previously described activation program, the information from the external storage device 20 is stored in the RAM 3 through the input means 4. Thus, the patch program is stored in a patch program portion of the RAM 3. However, the main program, the address of the first bug portion corresponding to the interrupt and vector data representative of the starting position of the patch program for patching the first bug portion are written in the fixed table area 31 of the RAM 3.

Accordingly, in this apparatus, in the beginning of the main program after activation, the address of the first bug portion in the main program and vector data representative of the starting position of the patch program for patching the first bug portion are read out from the fixed table area 31 of the RAM 3 and then written in the registers 7 and 8. Then, when the main program proceeds and the address thereof becomes coincident with the address of the register 7, a signal is supplied to the interrupt control portion X of the CPU 1.

Thus, data of the register 8 is referred to by the CPU 1 in processing of the interrupt control portion X, and a patch program located at the position indicated by the above data is executed. Further, at the end of this patch program, there are provided an address of the next patch portion of the interrupt program, vector data representative of the starting position of the patch program for patching the address, and a processing by which they are written in the registers 7 and 8, respectively. As described above, the patch portions of the main programs are patched sequentially.

According to the above-mentioned electronic apparatus, when the interrupt processings are requested in the interrupt control portions A, B, C, ..., the respective interrupt processings A, B, C, ... are executed. At the beginning of these interrupt programs, data written in the registers 7 and 8 are saved in the stack area 32 of the RAM 3. Further, the first patch portion address corresponding to the above interruption and the vector data representative of the starting position of the patch program for patching the address of the patch portion are read out from the fixed table area 31 of the RAM 3 and then written in the registers 7 and 8. As the interrupt program proceeds and the address becomes coincident with the address of the register 7, then a signal is supplied to the interrupt control portion X of the CPU 1.

Thus, the data in the register 8 is referred to by the CPU 1 for the interrupt processing and then

the patch program at the position indicated by that data is executed. Further, at the end of this patch program, there are provided an address of the next patch portion in the interrupt program and vector data representative of the starting position of the patch program for patching the address, and a processing by which they are written in the registers 7 and 8, respectively. In this way, the patch portions of the interrupt programs are sequentially patched. Furthermore, at the end of this interrupt program, data saved in the stack area 32 are written in the registers 7 and 8 one more time.

According to the above-mentioned electronic apparatus, when the interrupt processings are requested in the interrupt control portions A, B, C, ..., as shown in FIG. 4 of the accompanying drawings, the address of the patching portion of the main program and the vector data representative of the starting position of the patch program for patching the address are saved from the registers 7 and 8 to the stack area 32. Then, the address of the first patch portion corresponding to the above interrupt and the vector data representative of the starting position of the patch program for patching the address are read out from the fixed table area 31 of the RAM 3 and written in the registers 7 and 8. Thus, the patch portions of the interrupt programs are patched sequentially. Further, at the end of the interrupt program, the data saved in the stack area 32 are again written in the registers 7 and 8, whereby the patching process of the patch portions in the main program is continuously executed.

As described above, according to the above-mentioned electronic apparatus, the information stored in the fixed memory means (ROM 2) is patched by the information from the patch information memory means (RAM 3) and the information bug that is discovered when the electronic device was mass-produced can be patched. Also, by saving the discriminating data of the patch information to the stack memory (stack area 32), the bug can be patched during the interrupt.

Incidentally, in the above electronic apparatus, the stack area 32 may be arranged as a so-called pushdown stack. If so, then the electronic apparatus of the present invention can be applied to a multiple interrupt in which an interrupt is executed during an interrupt.

In the above-mentioned apparatus, the switching means for switching the memory access from the ROM 2 to the RAM 3 may be modified such that the vector data representative of the starting position of the patch program is replaced with a jump command to that position and the output data of the ROM 2 and the data in the register 8 is switched when the addresses compared by the comparator 9 become coincident with each other.

Further, in the above-mentioned apparatus, address data of the first patch portion corresponding to the interrupt is stored in the fixed table area 31 of the RAM 3 at every processing of various interrupts A, B, C, ... If there is no bug portion in an arbitrary interrupt processing, then corresponding data in the fixed table area 31 must be written in the fixed table area 31 by selecting an address which is not accessed during the interrupt processing.

However, in the above-mentioned apparatus, after the RAM 3 is cleared by the activation program and all data are cleared to "0", the information from the external storage device 20 is stored. Accordingly, when new data is not written therein, all addresses of the fixed table area 31 of the RAM 3 are all "0". On the other hand, addresses of "0" are assigned to the RAM areas in the CPU 1, this address can be inhibited from being accessed during the program processing. Therefore, if the arbitrary interrupt processing has no bug portion, then the above-mentioned object can be achieved by inhibiting new data from being written in the corresponding fixed table area 31 of the RAM 3.

According to the present invention, the information stored in the fixed memory means is patched by the information from the patch information memory means and the information bug that is discovered after electronic devices were mass-produced can be patched. Also, by saving the discriminating data of the patch portion into the stack memory, a bug can be patched during the interrupt processing.

Having described a preferred embodiment of the invention with reference to the accompanying drawings, it is to be understood that the invention is not limited to that precise embodiment and that various changes and modifications could be effected by one skilled in the art without departing from the spirit or scope of the invention as defined in the appended claims.

Claims

1. An electronic apparatus comprising:
   (a) fixed memory means (2) in which an information is stored in a fixed fashion;
   (b) address control means (1) for controlling an address;
   (c) input means (4) through which an external information is input;
   (d) patch information memory means (3) for storing therein a patch information concerning a portion to be changed in the information stored in the fixed memory means;
   (e) switching control means (7, 8, 9) for switching a memory access by the address control means from the fixed memory

means to the patch information memory means under the control of control data; and (f) wherein the address control means (1) includes a first memory in which there is saved the control data for controlling the switching of memory access by the address control means (1) when an interrupt processing is executed so that the control data for controlling the switching of the memory access during the interrupt processing can be set in the switching control means (7, 8).

2. The apparatus according to claim 1, wherein the fixed memory means (2), the address control means (1), the input means (4), the patch information memory means (3) and the switching control means (7, 8, 9) are unitarily integrated in a single chip in the electronic apparatus (10).

3. The apparatus according to claim 1 or 2, wherein the switching control means (7, 8, 9) includes a second memory (7) for storing therein address and data of a content to be patched.

4. The apparatus according to claim 3, wherein the second memory (7) is a register.

5. The apparatus according to anyone of claims 1 to 4, wherein the switching control means (7, 8, 9) includes comparing means (9) for comparing a present address with an address of the content to be patched.

6. A fixed information patching method for an electronic apparatus which comprises fixed memory means (2) in which an information is stored in a fixed fashion, address control means (1) for controlling an address, input means (4) through which an external information is input, patch information memory means (3) for storing therein a patch information concerning a portion to be changed in said information stored in said fixed memory means (2), and switching control means (7, 8, 9) for switching the memory access by said address control means (1) from said fixed memory means (2) to said patch information memory means (3) at a predetermined address, said method comprising the steps of:

saving control data for controlling the switching of the memory access by the address control means (1) to a first memory during the beginning of an interrupt processing to said address control means (1);
and

setting the control data for controlling the switching of the memory access during the interrupt processing in said switching control means (7, 8, 9).

7. The method according to claim 6, wherein the method steps are carried out with respect to a single integrated circuit chip in the electronic apparatus (10) in which the fixed memory means (2), the CPU (1), the input means (4), the random access memory (3) and the switching control means (7, 8, 9) are unitarily integrated.

8. The method according to claim 6 or 7, further including the step of storing address and data of a content to be patched in a second memory (7) in the switching control means (7, 8, 9).

9. The method according to claim 8, wherein the second memory (7) is a register.

10. The method according to anyone of claims 6 to 9, wherein the switching control means includes comparing means for comparing a present address with an address of the content to be patched.

11. A method of patching faulty information of a main program and interrupt programs for an electronic apparatus (10) in which the faulty information is stored in a read only memory (ROM) (2), read out to a random access memory (RAM) (3) and processed by a central processing unit (CPU) (1) of a single integrated circuit chip microcomputer, comprising the steps of:

(a) from an external memory source (20), writing into a patch program portion of the RAM (3), within the microcomputer, a patch program for patching the faulty information and writing into a fixed table area (31) of the RAM (3) an address of a first bug portion corresponding to an interrupt and vector data representative of a starting position of the patch program for patching the first bug portion;

(b) reading out the address of the first bug portion in the main program and vector data representative of the starting position of the patch program for patching the first bug portion from the fixed table area (31) of the RAM (3) and then writing the address of the first bug portion and the vector data in a patch address register (7) and a patch vector register (8), respectively;

(c) beginning processing of the main program and interrupting the processing by the CPU (1) of the main program when an ad-

dress called for by the main program is coincident with the address in the patch address register (7);
(d) after step (c), referring to the vector data of the patch vector register (8) for further processing by the CPU (1) and executing a patch program located at the position indicated by the vector data in the patch vector register (8);
(e) at the end of the patch program, writing in the patch address register (7) an address of a next patch portion of an interrupt program and writing in the patch vector register vector (8) data representative of a starting position of the next patch program for patching an address;
(f) interrupting the processing of the main program to process an interrupt program, and at the beginning of the interrupt program saving data written in the patch address register (7) and the patch vector register (8) in a stack area (32) of the RAM (3), reading out from the fixed table area (31) of the RAM (3) a first patch portion address corresponding to the interruption and a vector data representative of a starting position of a patch program for patching an address of the patch portion and then writing in the patch address register (7) the read out first patch portion address corresponding to the interruption and writing in the patch vector register (8) the read out vector data representative of a starting position of a patch program for patching an address of the patch portion;
(g) during the processing of the interrupt program, when an address specified by the CPU (1) is coincident with the address stored in the patch address register (7), supplying a signal to an interrupt control portion of the CPU (1) and causing the CPU to refer to the vector data in the patch vector register (8) for the interrupt processing and then execute the patch program at the position indicated by the vector data in the patch vector register (8);
(h) at the end of the patch program for the interrupt program, writing into the patch address register (7) an address of the next patch portion in the interrupt program and writing into the patch vector register (8) vector data representative of the starting position of the patch program for patching the address, whereby the patch portions of the interrupt programs are sequentially patched;
(i) at the end of the interrupt program, writing the data saved in the stack area (32) into the patch address register (7) and the patch vector register (8) once again, whereby a patching process of the patch portions in the main program is continuously executed.

12. An electronic apparatus comprising:
a central processing unit (CPU) (1);
a read only memory (ROM) (2);
a random access memory (RAM) (3);
an input port (4);
a data bus (5);
an address bus (6);
a patching portion address register (7) connected to the data bus (5);
a patching interrupt vector register (8) connected to the data bus (5);
a comparator (9) connected to the address bus (6) and to the patching portion address register (7) for detecting a coincidence between an address stored in the patching portion address register (7) and an address on the address bus (6) and for supplying an interrupt to an interrupt control portion of the CPU (1) which is also supplied with other interrupts for other processing, and for thereafter causing the CPU (1) to process program data specified by vector data stored in the patching interrupt vector register (8);
an external storage device (20), connected to the input port (4), for supplying a main program bug patching program and an interrupt program bug patching program;
wherein the CPU (1) stores the main program bug patching program and the interrupt program bug patching program in the RAM (3) and stores in a fixed table area (31) of the RAM (3) a first patch portion address corresponding to an interruption and a vector data representative of a starting position of a patch program for patching an address of the patch portion;
wherein the CPU (1) reads from the fixed table area (31) of the RAM (3) the first patch portion address corresponding to an interruption and the vector data representative of the starting position of a patch program for patching the address of the patch portion and writes in the patching portion address register (7) the first patch portion address corresponding to the interruption and writes into the patching interrupt vector register (8) the vector data representative of the starting position of a patch program for patching the address of the patch portion;
wherein the CPU (1) saves to a stack area (32) of the RAM (3) data written in the patching portion address register (7) and the patching

interrupt vector register (8), so that patching of program bugs can be carried out even during an interrupt.

FIG. 1

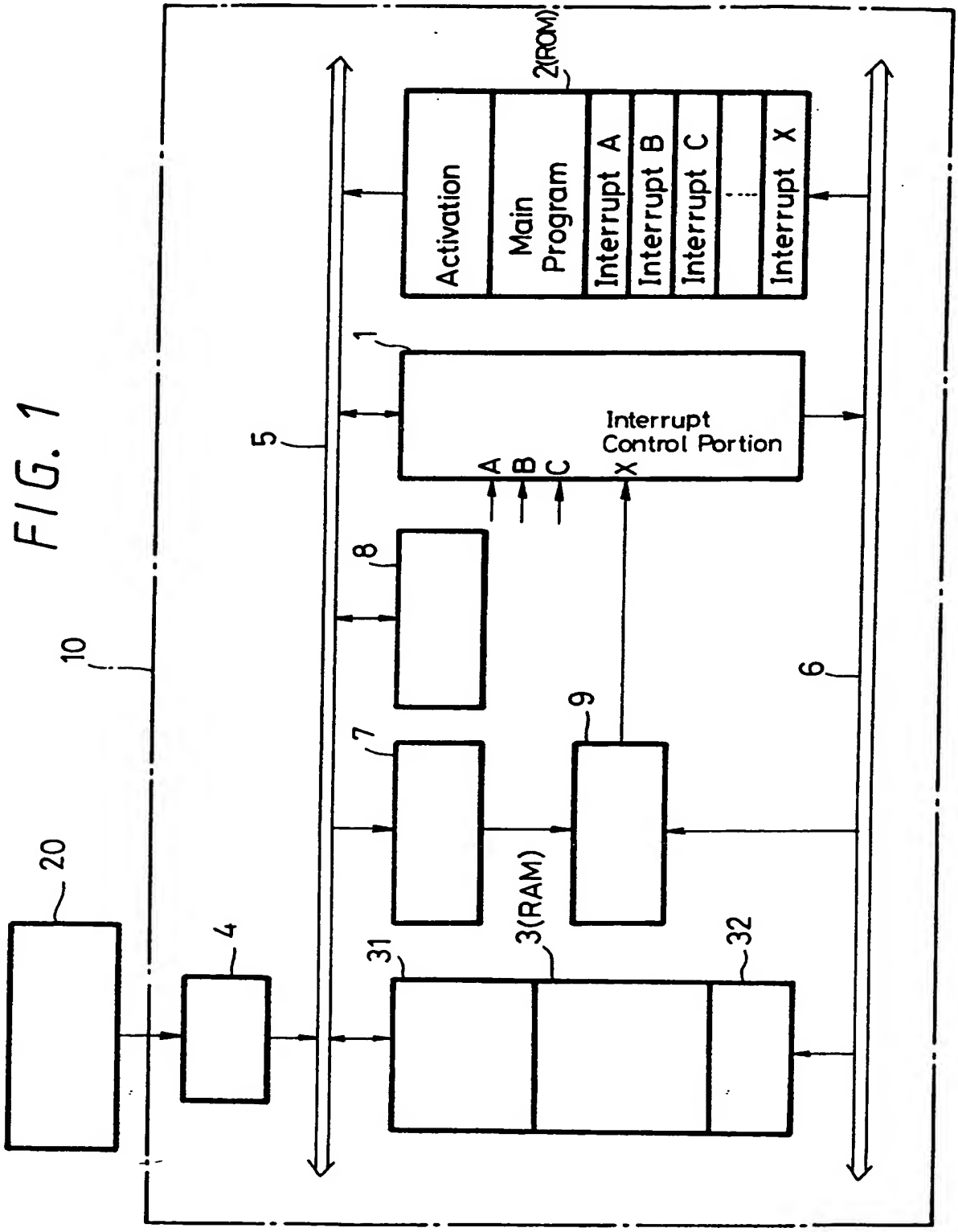

2(ROM)
Activation
Main Program
Interrupt A
Interrupt B
Interrupt C
Interrupt X
1
Interrupt Control Portion
A
B
C
X
5
8
10
6
9
7
20
4
3(RAM)
31
32

FIG. 2A

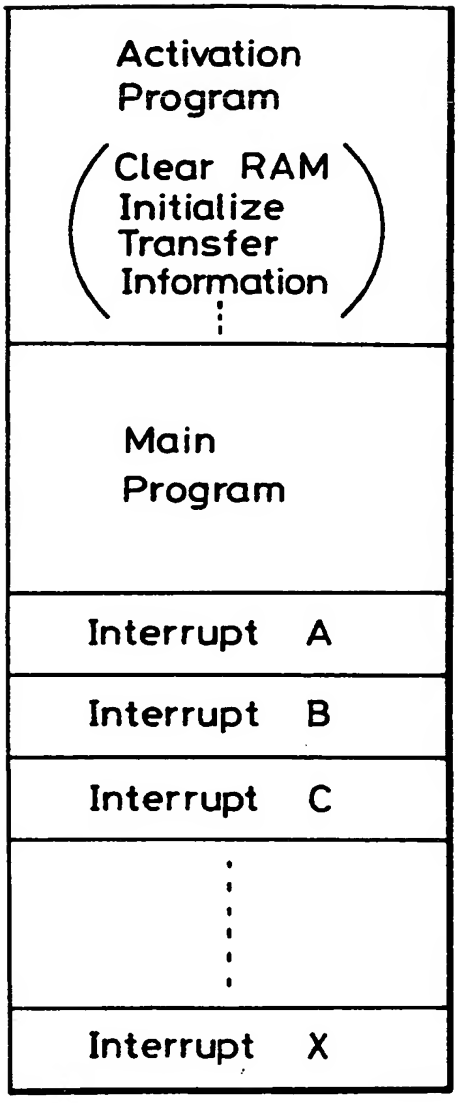

Activation Program
Clear RAM
Initialize
Transfer
Information
Main Program
Interrupt A
Interrupt B
Interrupt C
Interrupt X

FIG. 2B

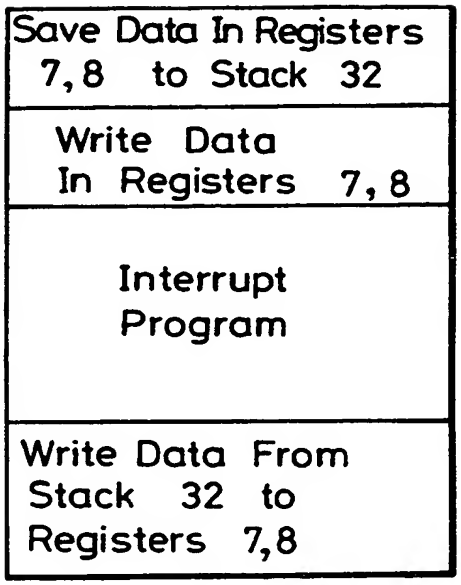

Save Data In Registers 7,8 to Stack 32
Write Data In Registers 7,8
Interrupt Program
Write Data From Stack 32 to Registers 7,8

FIG. 3

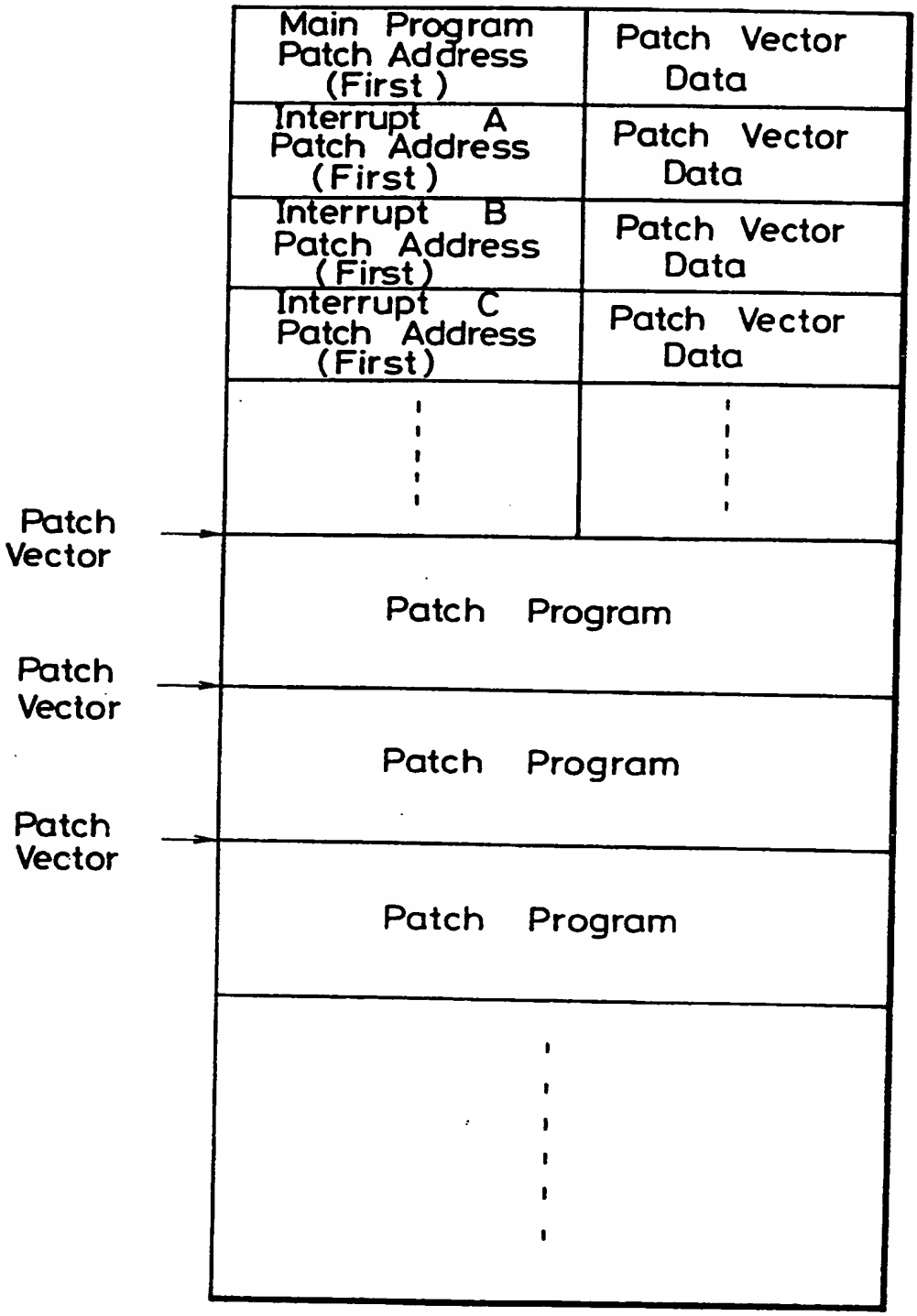
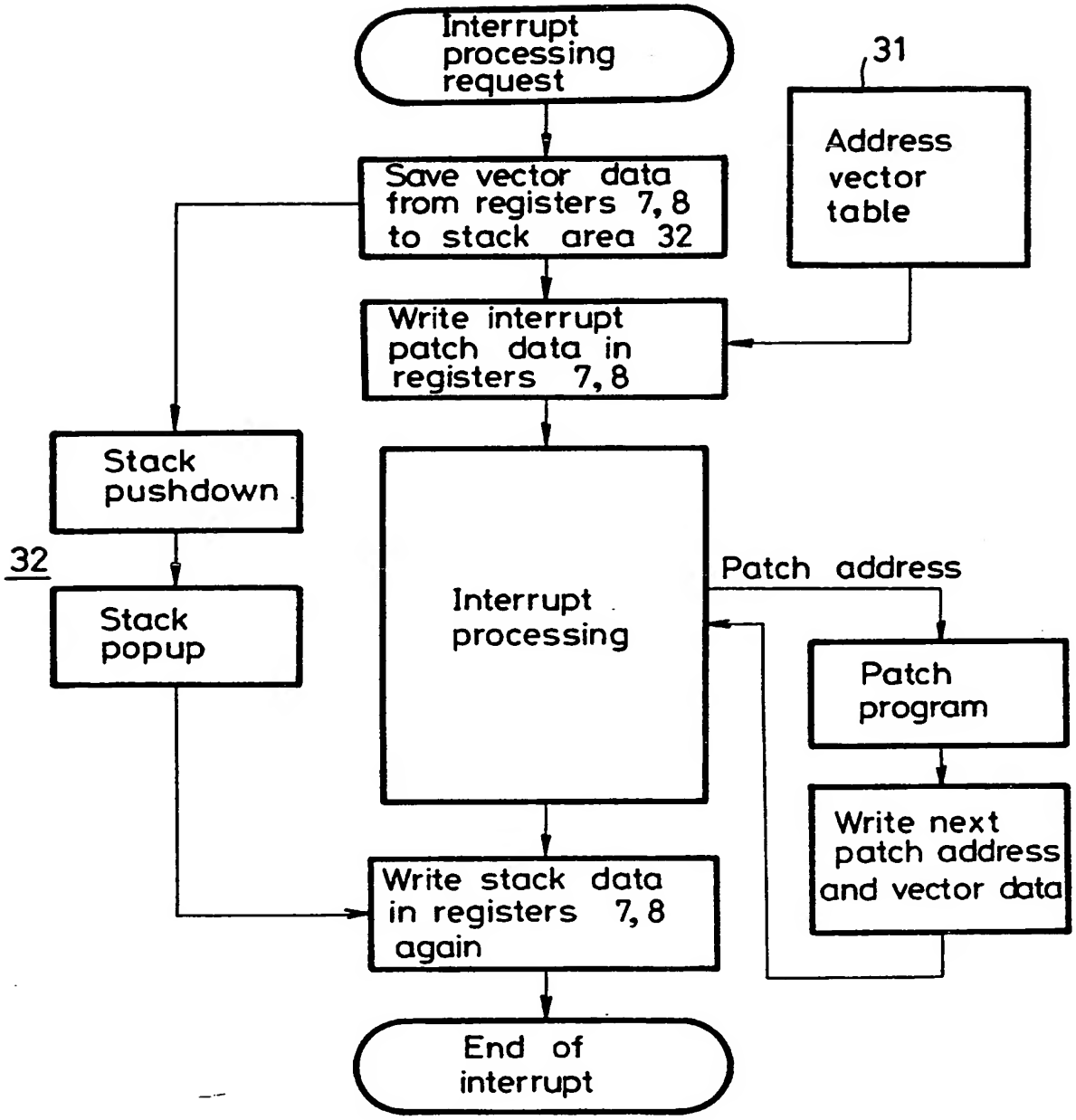

Main Program Patch Address (First)
Patch Vector Data
Interrupt A Patch Address (First)
Patch Vector Data
Interrupt B Patch Address (First)
Patch Vector Data
Interrupt C Patch Address (First)
Patch Vector Data
Patch Vector
Patch Program
Patch Vector
Patch Program
Patch Vector
Patch Program

FIG. 4


Interrupt processing request
31
Address vector table
Save vector data from registers 7, 8 to stack area 32
Write interrupt patch data in registers 7, 8
Stack pushdown
32
Stack popup
Interrupt processing
Patch address
Patch program
Write next patch address and vector data
Write stack data in registers 7, 8 again
End of interrupt

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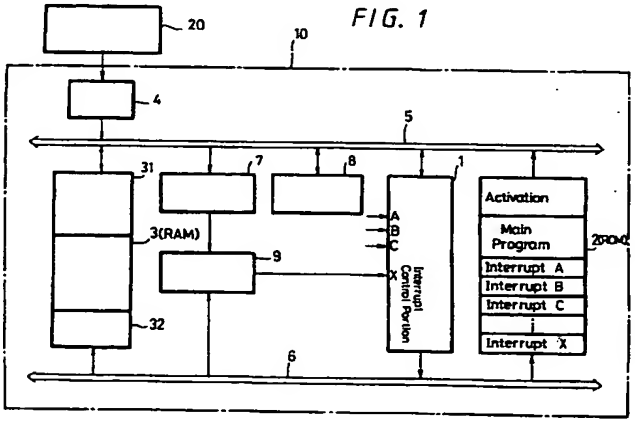
(54) Electronic apparatus and method for patching a fixed information

(57) An electronic apparatus (10) which includes a CPU (1), a ROM (2), a RAM (3), an input port (4), a data bus (5), an address bus (6), a patching portion address register (7) and a patching interrupt vector register (8) which are connected to the data bus (5), a comparator (9) which compares a coincidence with the address stored in the address register (7) and an address on the address bus (6) and supplies an interrupt to an interrupt control portion of the CPU (1) which is also supplied with other interrupts for other processing. Further, an external storage device (20), connected to the input port (4), supplies a main program bug patching information which is stored in the RAM (3), which includes a stack area (32) in which there are saved data written in the address register (7) and the patching interrupt register (8), so that patching of program bugs can be carried out even during an interrupt.

FIG. 1



EP 0 553 733 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 10 1008

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
Y	EP 0 458 559 A (SCHLUMBERGER INDUSTRIES LIMITED) * abstract * * column 1, line 40 - column 2, line 30 * * column 3, line 28 - column 6, line 19 *	1-12	G06F11/20 G06F9/26
Y	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 22, no. 1, 1979, ARMONK, USA, pages 350-352, XP002037473 "Read-Only Store Patching Methodology" * the whole document *	1-12	
A	US 4 802 119 A (HEENE ET AL.) * column 4, line 34 - line 51 * * column 5, line 3 - line 51 * * column 7, line 16 - line 42; figure 4 *	1-12	
A	US 4 607 332 A (GOLDBERG) * the whole document *	1	
A	ELECTRO, vol. 11, 1986, LOS ANGELES, CA, USA, pages 1-9, XP000211768 C. MELEAR: "APLLICATIONS FOR MICROCOMPUTERS WITH E2PROM"		TECHNICAL FIELDS SEARCHED (Int.Cl.5) G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12 August 1997	Absalom, R

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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